

Faculty Awards for Research

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LOW-POWER RF SOI-CMOS TECHNOLOGY FOR DISTRIBUTED SENSOR NETWORKS

INTRODUCTION

The objective of this work is to design and develop a silicon-on-insulator (SOI) CMOS chip for wireless data transmission/communication. The identified tasks for the first year in the FAR proposal included: (1) Identification of the receiver architecture, (2) Model development and technology characterization, and (3) Preliminary design of the low-noise amplifier (LNA). We report on the progress made in these areas and status of student support/advisement.

ACCOMPLISHMENTS

In the following we report on the accomplishments:

Identification Of The Receiver Architecture

RF Receiver must accomplish the following tasks: (a) Select the desired radio channel and reject other radio signals, (b) Amplify the desired radio signal and translate them back to baseband, and (c) Detect and decode the information with Low BER. In order to minimize cost and achieve high level of integration, receiver architecture should use least number of external filters, passive components. It should also consume least amount of power to minimize battery cost, size, and weight. One of the most stringent requirements for deep-space communication is the low-power operation. Our study identified that two candidate architectures listed in the following meet these requirements: (1) Low-IF receiver, (2) Subsampling receiver. The low-IF receiver uses minimum number of external components. Compared to Zero-IF (Direct conversion) architecture, it has less severe offset and flicker noise problems. The Subsampling receiver amplifies the RF signal and samples it using track-and-hold Subsampling mixer. These architectures provide low-power solution for the short- range communications missions on Mars.

Model Development And Technology Characterization

RF circuit design requires accurate device models for active and passive components. On-chip inductive elements (inductors and transformers) are commonly used in low-noise amplifiers and VCO's. Public domain software developed at UC Berkeley, ASITIC, is used for prediction and optimization of the on-chip inductive elements. ASITIC allows circuit and process engineers to design and optimize the geometry of on-chip inductive devices and the IC process parameters affecting their electrical characteristics. We have downloaded and configured ASITIC on our Unix Server. We also use built-in inductor and transformer models available in Spectre RF that is the analog circuit simulation tool in CADENCE VLSI design environment. Spectre RF has built in device models for MOSFETs that are accurate for the frequencies used in this work.

Preliminary Design Of The Low-Noise Amplifier (LNA)

The first stage of a receiver is typically a low-noise amplifier, whose main function is to provide enough gain to overcome the noise of subsequent stages. LNA should also accommodate large signals without

distortion, and present 50-Ohm impedance to the input source (i.e. antenna). Due to its ability to reject common-mode disturbances such as substrate noise, Differential LNA architecture was chosen for this work. Source inductor degeneration is used to realize 50 Ohm input impedance. One of the most important requirements for the deep-space short-range communication is the low-power requirement. We used fixed-power optimization in the design. In this approach, noise figure of the LNA is optimized for fixed power dissipation. Constant- g_m biasing technique is used for the biasing currents of the LNA. Biasing circuit provides stability against bias voltage and temperature variations. The LNA was designed using 0.5-micron CMOS process available through MOSIS. LNA consumes 12 mW power and provides 18 dB gain with 2.3 dB noise figure. Die area required by the LNA is 1.8 mm by 1.4 mm. Due to low resonance frequency (400 MHz), on-chip inductors used in the LNA are much larger compared to LNA's designed for 900 MHz and beyond. We are investigating the use of capacitive loading to decrease the required inductance values at UHF frequencies. We are also investigation other circuit architectures that do not require on-chip inductance.

RELEVANCE TO NASA STRATEGIC ENTERPRISES

This work directly contributes to the "Human Exploration and Development of Space Enterprise". Micro Communication and Avionics Systems (MCAS) program at JPL requires development of low-mass/low-power microelectronics components for deep-space communications. SOI-CMOS technology under development will find use in missions to Mars and other Planets providing communication between distributed sensors, orbiter and lander.

BENEFITS TO SOCIETY

This work advances the state-of-the-art in SOI CMOS technology that has commercial and military applications. SOI CMOS technology provides "competitive advantage" to the Unites States. It also provides hands-on research experience to minority students in CMOS integrated circuits.

STUDENT ACHIEVEMENTS

One of the main objectives of NASA FAR project is to increase participation of minority students in research and provide training for undergraduate and graduate students. Five students received financial support and research experience/training as a result of this project. Students participated in the "NASA Day" that was held on North Carolina A&T State University Campus. Students successfully completed the design of a CMOS UHF low-noise amplifier. They are submitting journal/conference papers on their research work.